



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,257	12/02/2003	Gary Shipton	PEA11US	6710
24011	7590	04/05/2006	EXAMINER	
SILVERBROOK RESEARCH PTY LTD			PATEL, HARI	
393 DARLING STREET			ART UNIT	
BALMAIN, NSW 2041			PAPER NUMBER	
AUSTRALIA			2115	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/727,257

Applicant(s)

SHIPTON ET AL.

Examiner

Hari Patel

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/02/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 5 are presented for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed 12/02/04 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the documents cited therein do not appear to be relevant to the patentability of the instant claimed invention. The IDS has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

4. There are 331 sheets of Drawings and at least 413 figures. The drawings must show every feature of the invention specified in the claims. See 37 CFR 1.83(a). Applicant is required to show where each and every claimed element or step is shown in the Drawings.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. The Specification is over 1000 pages long. Applicant is required to show the antecedent basis in the Specification for all claimed elements (i.e. the precise location of all claimed elements or steps).

8. Claim 2 – 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Art Unit: 2115

9. Claims 2 – 5 recite the limitation “An integrated circuit according to claim 1”. It is suggested this be changed to “The An integrated circuit according to claim 1”.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1, 2, and 4 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1 and 2 of copending Application No. 10/727238 (hereinafter referred to as ‘238). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Art Unit: 2115

- Claim 1 of the instant application is nearly identical to the limitations of Claim 1 of '238, wherein the differences are:
 - the element "non-volatile memory" (claim 1, line 1) of the instant application is essentially identical to the element portion "a memory" (claim 1, line 1) of '238) and would have been obvious because the "memory" disclosed in '238 must essentially be non-volatile;
 - the element "power supply" (claim 1, line 2) of the instant application is essentially identical to the element portion "external power source" (claim 1, line 3) of '238 and would have been obvious because both elements are sources of power;
 - the element "the integrated circuit is configured to enable multi-word writes to the non-volatile memory" (claim 1, lines 2-3) of the instant application would have been obvious because claim 1 of '238 discloses circuitry used for writing address and data values to memory, wherein address and data values are multi-word writes; and
 - the element "preventing subsequent words in any multi-word write currently being performed from being written to memory" (claim 1, lines 5-6) would have been obvious because '238 discloses "ability to alter data in the memory is disabled prior to address or data

values to be written to the memory becoming unreliable due to failing power" (claim 1, lines 6-8). Since data cannot be altered

- Claim 2 of the instant application is nearly identical to the limitations of claim 1 of the instant application and would have been obvious because claim 1, lines 5-6 of '257 recite "in the event the quality of the power drops below a predetermined threshold, preventing subsequent words in any multi-word write currently being performed from being written to memory.
- Claim 4 of the instant application is nearly identical to the limitations of claim 2 of '238 and would have been obvious because claim 3 of the instant application discloses, "wherein the memory is flash memory" while claim 2 of '238 discloses "wherein the memory is flash memory".

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2115

13. Claims 1 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walmsley (U.S. PG-Pub No. 2004/0236961) and further in view of Muller (U.S. Patent No. 4,644,494)..

14. As per Claim 1, Walmsley teaches an integrated circuit (*Abstract, claim 1, and claim 18*) comprising a processor, (*paragraph [0738], lines 7-11*), non-volatile memory (*claims 1 and 18*), an input power supply line (*claim 1*), inherently requiring a power supply not explicitly disclosed, and a power detection unit (*claim 1 – detection unit and claim 18 – power supply monitoring circuitry*), wherein the integrated circuit is configured to enable multi-word writes to the non-volatile memory (*paragraph [0576], lines 13-14*), the power detection unit being configured to:

monitor a quality of power supplied to the input (*claim 18, lines 6-8*);

15. Walmsley, however, does not teach that in the event the quality of the power drops below a predetermined threshold, preventing subsequent words in any multi-word write currently being performed from being written to the memory. Specifically, Walmsley teaches that in the event the quality of power drops below a predetermined threshold (*claim 21*), the power supply monitor is configured to cause deletion overwriting, or otherwise rendering unreadable data in the memory. Walmsley fails to teach the inhibiting of any further words of a multi-word write to be written into memory once power drops below a specific threshold.

Art Unit: 2115

16. Muller teaches an apparatus comprising a processor (*Fig. 1 – Central Processing Unit, 24*), non-volatile memory (*Fig. 1 – Memory Unit [EEPROM], 38 and col. 8, lines 15-16*), and input for receiving power from a power supply (*Fig. 1 – Power Supply, 30*) and a power detection unit (*Fig. 1 – Power Monitor, 52*), wherein the apparatus is configured to enable multi-word writes to the non-volatile memory (*col. 3, lines 19-22*), the power detection unit configured to:

monitor a quality of power supplied to the input (*col. 2, lines 29-51*);

in the event the quality of the power drops below a predetermined threshold, preventing subsequent words in any multi-word write currently being performed from being written to the memory (*col. 9, lines 49-54 and col. 3, lines 20-22*).

17. It would have been obvious to one of ordinary skill in the art to combine the teachings of Walmsley and Muller because they both teach a circuit configured to monitor the quality of power supplied to the circuit to monitor if the voltage level drops below a predetermined threshold. Muller's disclosure of an apparatus for preventing subsequent data to be written to memory after the power level dropping below a predetermined threshold would prohibit erroneous data from being written to memory.

18. As per Claim 2, Muller teaches the circuit further configured to prevent any further writes of any type to the memory once the quality is determined to have dropped below the threshold (*col. 2, lines 29-51 and col. 9, lines 49-54*).

Art Unit: 2115

19. As per Claim 3, Walmsley teaches the integrated circuit, wherein the quality is a voltage (*claim 19*). Muller also teaches the circuit, wherein the quality is a voltage (*col. 9, line 52*).

20. As per Claim 4, Muller teaches the circuit, wherein the memory is EEPROM (*col. 8, line 15-16*). It is known in the area of the pertaining art that flash memory is a type of EEPROM.

21. As per Claim 5, Muller teaches the claimed circuit according to Claim 1 as mentioned above. It would have been obvious to one of ordinary skill in the art that a reset signal be provided from the power detection unit to at least some other circuits on the circuit once any current writes have been finished. See Germer (U.S. Patent No. 4,999,575 – col. 15, lines 18-27); Sakagami et al. (U.S. Patent No. 5,233,557 – col. 4, lines 23-27); McClure (U.S. Patent No. 5,619,456 – col. 23, lines 9-12); and Kimura et al. (U.S. Patent No. 5,655,076 – col. 7, lines 51-54).

Conclusion

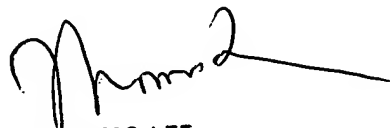
22. Any inquiry concerning this communication from the examiner should be directed to Hari Patel whose telephone number is 571-272-2743. The examiner can normally be reached on Monday – Thursday from 8:00am – 5:30pm and every other Friday from 8:00am – 4:30pm.

Art Unit: 2115

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee, can be reached at 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of the application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Hari Patel
Examiner
Art Unit 2115



THOMAS LEE
SENIOR PATENT EXAMINER
TECHNOLOGY CENTER 2100